REMARKS

Reconsideration of the above-referenced application in view of the above amendment, and of the following remarks, is respectfully requested.

Claims 1-10 are pending in this case. Claims 11-20 are cancelled herein.

The Examiner rejected claim 1 under 35 U.S.C.§ 103(a) as being unpatentable over Shiba et al., Dunaway et al., or Grzyb et al.

Applicant respectfully submits that claim 1 is patentable over Shiba et al, Dunaway et al and Grzyb et al as there is no disclosure or suggestion in any of these references of an integrated circuit comprising an on-chip decoupling capacitor located over a topmost metal interconnect level, as required by claim 1. Shiba et al teaches a capacitor formed between the power and ground wirings. Shiba does not disclose or suggest a decoupling capacitor located over a topmost metal interconnect level as the capacitor is taught and shown as being formed below metal interconnect 7. Dunaway teaches an off-chip decoupling capacitor mounted on the leadframe rather than an on-chip decoupling capacitor as claimed. Grzyb teaches a capacitor between the first two metal interconnects (IN and INS) and teaches that the capacitor should be formed as close to the cell as possible. Grzyb does not disclose or suggest a decoupling capacitor located over the top most metal interconnect level. Accordingly, Applicant respectfully submits that claim 1 is patentable over the references.

The Examiner rejected claims 2-10 under 35 U.S.C.§ 103(a) as being unpatentable over Ohtsuki in view of Saito et al, and also in view of Urdahl et al., Kar-Roy et al., and Armacost et al.

Applicant respectfully submits that claim 2 is patentable over Ohtsuki in view of Saito and also in view of Urdahl, Kar-Roy and Armacost as there is no disclosure or

suggestion in the references of a topmost metal interconnect level located over a lower metal interconnect level, the topmost metal interconnect level comprising a first and a second metal interconnect line, a bottom electrode located over and in electrical contact with the first metal interconnect line, a capacitor dielectric located over the bottom electrode, and a top electrode located over said capacitor dielectric. Ohtsuki teaches a memory cell capacitor formed above the substrate but below at least one metal interconnect 118. While metal interconnect 118 is not illustrated in Figure 9, the capacitor is also located below third metal interconnect 16. The memory cell capacitors of Ohtsuki are located below at least one metal interconnect 118, 115, 16 rather than over a topmost metal interconnect level as required by the claim. Saito is added to teach connecting the plate line of a memory cell to ground in a dummy cell. Urdahl teaches a TaN capacitor electrode. Kar-Roy teaches a Hafnium-oxide and silicon nitride for a capacitor dielectric. Armacost teaches a copper interconnect. Accordingly, Applicant respectfully submits that claim 2 and the claims dependent thereon are patentable over the references.

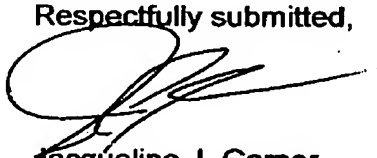
Regarding claims 3 and 4, Ohtsuki clearly teaches the layer 16 is a third metal interconnect layer. The fact that a metal interconnect may comprise aluminum, does not negate the fact that layer 16 is a metal interconnect layer. Thus, the bottom electrode is not located over a topmost metal interconnect as required by claim 2, from which claims 3 and 4 depend. Furthermore, while layers 14, 15, and 16 do connect a top electrode to an interconnect line it is not a second interconnect line of the same topmost interconnect level as the bottom electrode is connected to, as required by claim 3. Accordingly, Applicant respectfully submits that claims 3 and 4 are further patentable over the references.

Applicant respectfully submits that claim 9 is patentable over the references as there is no disclosure or suggestion in the references of a topmost copper interconnect level comprising a first and a second copper interconnect line, a bottom electrode in direct contact with the first copper interconnect line, a capacitor dielectric, a top electrode, a protective overcoat located over the topmost copper interconnect level, and

an aluminum cap layer located, in part, over the protective overcoat and electrically connecting the top electrode and the second copper interconnect. Ohtsuki fails to teach a bottom electrode in direct contact with the first copper interconnect line and an aluminum cap electrically connecting the top electrode and the second copper interconnect, wherein both the first and second copper interconnect lines are part of the same topmost copper interconnect level. Furthermore, the references fail to teach the recited combination of aluminum cap as connected and copper interconnect. Accordingly, Applicant respectfully submits that claim 9 and the claim dependent thereon are patentable over the references.

In light of the above, Applicant respectfully requests withdrawal of the Examiner's rejections and allowance of claims 1-10. If the Examiner has any questions or other correspondence regarding this application, Applicant requests that the Examiner contact Applicant's attorney at the below listed telephone number and address.

Respectfully submitted,



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